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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/727,440 | 12/04/2003 | Ken G. Pomaranski | 200209695-1 | 6842 |

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| EXAMINER | |
|---|---|
| BUI, BRYAN | |
| **ART UNIT** | **PAPER NUMBER** |
| 2863 | |

DATE MAILED: 03/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/727,440 | POMARANSKI ET AL. | |
| | Examiner | Art Unit | |
| | Bryan Bui | 2863 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11 and 13-19* is/are rejected.

7)☒ Claim(s) *10,12 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date R403
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-9, 11, 13-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Nejedlo et al. (US20040117709).

With respect to claims 1, 13 and, 17, Nejedlo et al teach a computer system having an interconnect test module comprising a processor configured to cause an operating system to be booted (paragraph 0029); an interconnect (paragraph 0030), a first test unit coupled to the interconnect, and a second test unit coupled to the interconnect (figure 3, paragraph 0041); wherein the first test unit is configured to provide a test pattern to the second test unit on the interconnect in response to a (first) signal from the operating system (paragraphs 0038, 0041). Nejedo et further discloses the second test unit is configured to detect an error in the interconnect in response to receiving the test pattern and notifying (indicating, reporting) the operating system in response to detecting an error (paragraphs 0034).

With respect to claims 2-9, 11, 14-16, Nejedlo et al teach the second test unit is configured to detect an error in the interconnect in response to receiving the test

pattern, wherein the second test module is configured to provide a second test pattern to the first test module, the first test module is configured to detect an error on the interconnect in response to receiving the second test pattern, wherein the operating system is configured to provide the first signal to the first test module in response to detecting a second signal from the first test module, first component comprise a processor, and the second component comprises a controller having system and memory controller coupled to the processor, and I/O controller/device , an expansion slot (paragraphs 0023, 0028, 0034, 0041, figures 1A-B, 2).

With respect to claims 18-19, Nejedlo et al further disclose a first switching and second switching coupled to first test unit and second test unit, wherein first test configured to cause the switch to connect to the first test unit to the interconnect and the second test unit is configured to cause the second switch to connect to the second test unit to the interconnect; a first component coupled to the first switch and a second component coupled to the second switch, wherein the first test unit is configured to cause the first switch to disconnect the first component from the interconnect, and the second test unit is configured to cause the second switch to disconnect the second component from the interconnect (paragraphs 0041, claims 5,7, 17).

3. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Ellis et al. (US20040117708).

With respect to claim 1, Ellis et al teach a computer system having an interconnect test module (figures 1, 2) comprising a processor (108) configured to cause an operating system to be booted (paragraph 0005); an interconnect, a first test

unit coupled to the interconnect, and a second test unit coupled to the interconnect (figure 2); wherein the first test unit is configured to provide a test pattern to the second test unit on the interconnect in response to a (first) signal from the operating system (paragraphs 0005, 0019, 0021, 0022).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 13 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellis et al (US20040117708) in view of Nejedo et al (US20040117709).

Ellis et al disclose a computer system having an interconnect test module (figures 1, 2) comprising a processor (108) configured to cause an operating system to be booted (paragraph 0005); an interconnect, a first test unit coupled to the interconnect, and a second test unit coupled to the interconnect (figure 2); wherein the first test unit is configured to provide a test pattern to the second test unit on the interconnect in response to a (first) signal from the operating system (paragraphs 0005, 0019, 0021, 0022). Ellis et al do not teach the second test unit is configured to detect an error in the interconnect in response to receiving the test pattern and notifying (indicating, reporting) the operating system in response to detecting an error. Nejedo et al teach these limitations in paragraphs 0034. It would have been obvious to one of ordinary skill in the art to modify the teachings of Ellis et al to include Nejedo et al'

technique to provide the system more accuracy in performing interconnect testing device in a computer system.

***Allowable Subject Matter***

6. Claims 10, 12, 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bryan Bui whose telephone number is 571-272-2271. The examiner can normally be reached on M-Th from 7am-4pm, and Alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BB

3/9/05

**BRYAN BUI**
**PRIMARY EXAMINER**